Abstract - From wafer sort to yield learning is a long, complex process. Even worst because when scan chains fail, wafer sort adds negligible value. To address this gap a fast, reliable and accurate localization technology for scan chain fails that enable rapid translation of these into yield learning is presented.

Summary and results:

Before shipment, wafer sort screens die. Sort analysis on failing die provides fault localization that contributes to yield learning. Sometimes Sort test can not be completed and as a result yield learning requires lengthy analyses of these die. Such cases seems to be increasing as process geometries continue to shrink.

Several questions arise:

• What are typical percentages of fails during product bring-up?
• Why might this be an increasing trend?
• What can be done if this trend is increasing?

Scan logic test is a very useful methodology to help localize failures in ICs. Logic test is a structural integrity (non-functional) test of the logic circuit using designed-in scan chains. Before logic testing, however, scan chain shift test is run to make sure the scan chain itself is working properly. When scan chain shift test fails, logic test can provide no information and therefore, does not contribute to yield learning. In this case, the practice has been to bypass all die with scan chain shift failures. This worked when the failing percentages were low but when scan chain shift failures are > 30% then too much valuable data is bypassed.

Note: the location of each scan chain is known at the design house and can be used to provide a coarse level of localization (See Fig 1).

With the optical imaging technique called Laser Voltage Imaging (LVI) and Laser Voltage Probing (LVP), the chain can be inspected and the failing flip-flop located.

The LVI laser scans the backside of the die and is reflected back to a detector (See Fig. 2). The incident beam is focused onto the active layer of the die so that the reflected beam provides physical details of the scanned active area—an LSM image (pattern image). Simultaneously during this scan, the reflected beam is modulated by the signal on each transistor in the scanned area. The high frequency component of the reflected signal is fed to a spectrum analyzer (SA) that is tuned to a specific frequency. The SA provides information in the frequency domain. Or the modulated signal is fed to an Oscilloscope to provide information in the time domain. If a transistor is toggling at the target specific frequency, then it is highlighted in the image, creating a spatial map of the target toggling frequency when overlaid onto the LSM image.
FIG 2. Laser Voltage Imaging (LVI) basic architecture, illustrating the simultaneous acquisition of the LSM IC image and the LVI guaranteeing their alignment.

The test engineer can then see at a glance if the transistors in that field of view match expected toggling behavior. Once a suspected transistor is identified further information can be collected using LVP (See Fig. 3).

Scan chain shift debug is a natural application for LVI and LVP, because a known frequency can be applied to the scan chain by looping a 1100… pattern or such into the scan chain data stream. Distinct frequencies become available for LVI analysis, the data frequency the clock frequency (4 x data frequency). Two spectrum analyzers, tuned to the desired frequency, further improve throughput, by collecting LVI for 2 individual frequencies simultaneously [1].

FIG 3. LVP waveforms provide a clear verification that data propagating through the scan chain is breaking down between flop 514 to 515. Flop 514 data is 11001100 as expected, however, flop 515 data is 01110111. Toggle/shift failure occurred between flop 514 and 515. LVP shows Flop 515 input and output as 11101110.

By scanning the laser over a field of view with sufficient resolution an area of the scan chain is examined. With a binary search the defect area is identified. Steps in a Binary Search are shown in Fig. 4.

For a 6000 flop chain generally 5 to 6 search steps are required to get close to the failing flip-flop. The first few search steps can be done very fast with 256 pixels per line resolution on a large field of view (FOV).

The last few steps of the search are a bit slower as we increase resolution (to 1024 pixels per line) but the scanned FOV can be reduced to conserve analysis time. The final verification of the failing flop is done by LVP. The waveform acquired clearly show data input and output of the flop in question. The test engineer can clearly see the failure location as well as verify the failure mode, stuck-at fault or toggle/shift failure (see Fig. 3 and 5).

FIG 4. Wafer-level time table for LVI scan chain debug with an average 6000-flop scan chain (32 nm process). Pink shows time saved when wafer utilizes the same card, interface, tester and map.

FIG 5. (32nm process) Scan Chain overlay with LVI data showing 2 flops 2290 and 2291 with LVI data at 3 different frequencies. The image on the Top shows CLK (10MHz) in red overlay and data (2.5MHz) as green overlay. The image on the bottom shows the same CLK (10MHz) in red but the data target frequency is set for 5MHz. We can clearly see that these flops are functioning normally with data of 2.5MHz (11001100) and have no toggle/shift failure as there is no 5MHz signal (11101110).
To do this at wafer sort, probe card probe to pad alignment (PTPA) is of course critical and is accomplished by viewing the probe-card pins (up to 10,000 pins are supported) and matching the probe card pins to the CAD layout of the device. Then registering the wafer pads/solder bumps to the CAD of the device thus matching the probe card pins to the wafer pads/solder bumps. A traditional probing wafer chuck can not be used because opto-mechanical components fill the space under the table top. The wafer backside area is visible to upward-looking system optics through a window in the table surface. A new scheme was implemented which uses the table top for wafer support and a wafer edge-gripping technique to retain the wafer for X/Y motion [2]. The probing system moves the Probe Card down to press on the wafer. The Probe Card is connected to the test head via a flexible interface, this eliminates the need for lengthy hard dock process as well as tester induced vibrations. The simple straightforward design of the system allows for very fast die to die indexing with no adjustment or realignments. This facilitates probing of multiple dies much faster than traditional methods of the past. Times for each step are shown in Fig. 4.

The challenging alignment, however, is that between the CAD Layout and the IC image (See Fig 6). When features in a 120μm field of view are too similar, such as a sea of gates, alignment becomes difficult at 28nm process technologies. Improved optics, which enables 190 nm resolution and automated CAD to Image Alignment, are addressing this challenge. The value of this approach is in its localization accuracy, its adaptability to automated binary search and overall increased analysis speed.

Successful physical failure analysis, PFA, at the defect site is > 90% and in general localization takes ~ 1 hr per scan chain. With this approach die that were once bypassed due to broken scan chains can contribute to yield learning thus shortening the overall yield ramp.

The following two case studies illustrate the solution based on LVI and LVP for rapid scan chain fault localization, suited for Logic devices. This work was done on full thickness wafers with no sample preparation and on multiple die per wafer.

**Case Study 1: Failing scan chain shift with a “stuck at” failure.**

LVI binary search was used to localize the failing Flop. (See Fig. 7).

![Fig 7: Lack of LVI activity on the failing flop, highlighted in Red.](image)

LVP was used to verify faulty flop is “stuck at” high or low. Looking at the waveforms clearly showed the failure mode as the flop being stuck. (See Fig. 8).

![Fig 8: The Faulty Flop, bottom trace is stuck—no switching activity. Top trace is what should be seen.](image)

Fan-Out/Fan-In Net analysis using NEXS Net Trace pointed to the suspected Poly Net (CAD Data can not be shown due to the proprietary nature of device layout). Final PFA confirmed a poly bridge. (See Fig. 9)

![Fig 9:](image)
Fig 9: SEM top view image shows the poly bridge.

**Case Study 2: Failing scan chain with a “Toggle” failure.**

LVI binary search used to localize the failing flop. In Toggle failure we are looking for a frequency which is the second harmonic of the data frequency. In this case data frequency was 2.5 MHz so the Spectrum Analyzer was set to look for 5 MHz LVI activity. In this example Red represents 2.5 MHz LVI activity and the green represents 5 MHz LVI activity. The failing flop highlighted in red showed strong LVI signal at 5 MHz but no signal at 2.5 MHz. (See Fig 10.)

Fig 10: Flop 515 is the first flop to show LVI signal at the second harmonic frequency of 5 MHz.

LVP was used to verify faulty flop. Looking at the waveforms clearly shows the failure mode was a toggle failure for which the expected 11001100 vector pattern became 11101110 (See Fig. 11).

Fig 11: LVP shows Flop 515 input and output as 11101110.

TEM plan-view image of the failed Flop shows an abnormal enlarged contact. It is about 7 nm larger compared to its neighboring contacts. A TEM slice was prepared further analysis showed missing TiN. Final EDX mapping is used to clearly show the missing Ti and N (See Fig. 12 and 13).

Fig 12: TEM plan-view image shows that contact 1 was abnormally large. Contact diameters of the bad contact as well as a typical good contact were recorded on the image.

Fig 13: EDX Mapping was used to identify partial missing TiN.
A TEM cross-section sample of an equivalent failure was prepared and analyzed, using EDX mapping to separate the elements and fully characterize the problem (See Fig. 14 and 15).

Fig 14: TEM cross-section micrograph shows the enlarged contact 1 on the right.

Fig 15: EDX Mapping clearly shows there is no TiN at the bottom of the enlarged contact 1.

Conclusion:
From wafer sort to yield learning is a long, complex process. Physical failure analysis (PFA) at the defect site using LVI has been > 90% successful. In general localization takes ~ 1 hr per scan chain. Wafer sort can now add more value so that with this LVI approach, die that were once bypassed due to broken scan chains contribute to yield learning thus shortening the overall yield ramp. LVI is a fast, reliable and accurate localization technology for scan chain shift fails that enable rapid translation of these into yield learning.

References: